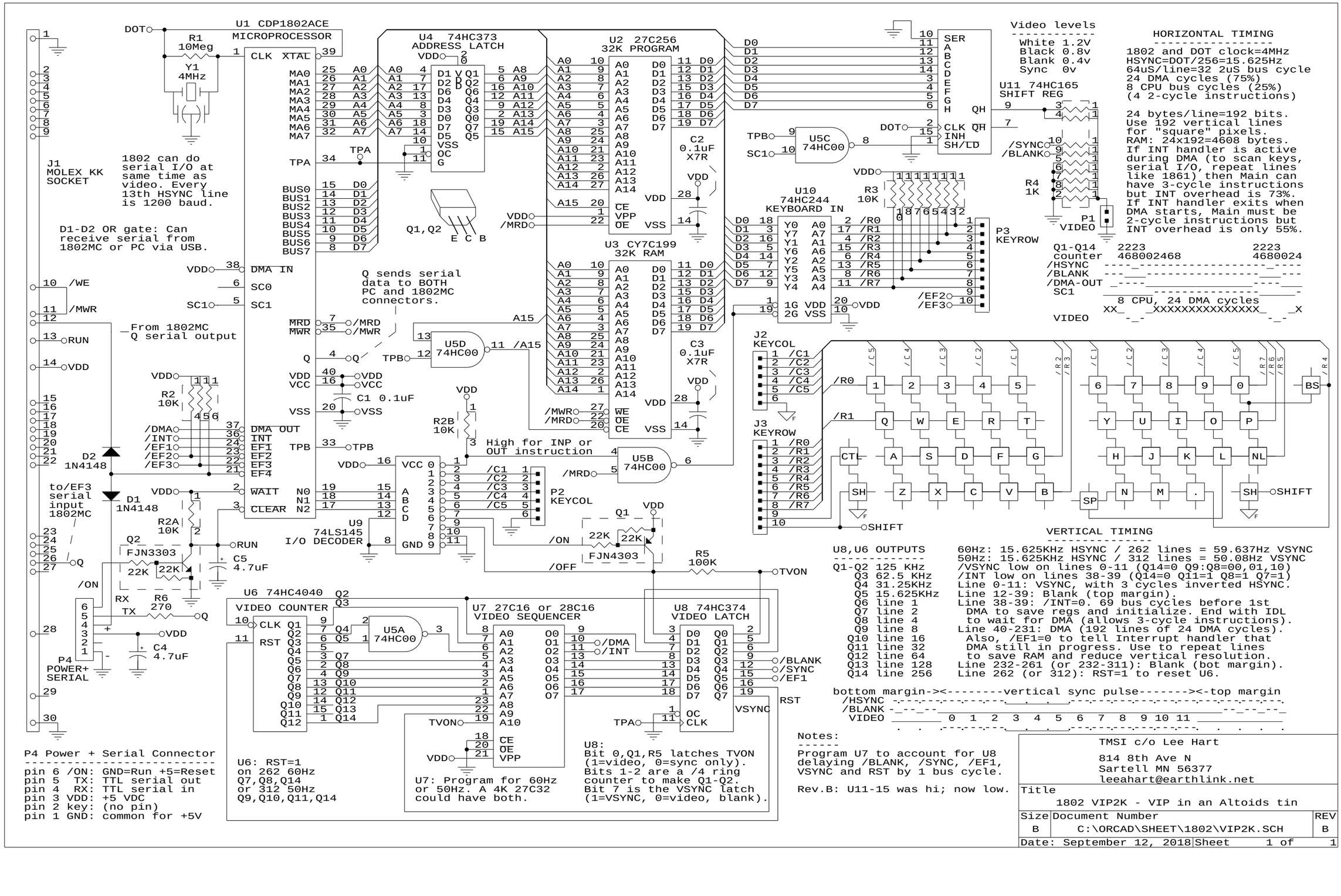
U1 CDP1802ACE
MICROPROCESSOR
R1
10Meg
Y1
4MHz
DOT
CLK
XTAL
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
TPA
BUS0
BUS1
BUS2
BUS3
BUS4
BUS5
BUS6
BUS7
J1
MOLEX KK
SOCKET
1802 can do serial I/O at same time as video. Every 13th HSYNC line is 1200 baud.
D1-D2 OR gate: Can receive serial from 1802MC or PC via USB.
U4 74HC373
ADDRESS LATCH
U2 27C256
32K PROGRAM
U3 CY7C199
32K RAM
C2
0.1uF
X7R
C3
0.1uF
X7R
Q1,Q2
E C B
VDD
/MRD
A15
Q sends serial data to BOTH PC and 1802MC connectors.
From 1802MC
Q serial output
/WE
/MWR
RUN
VDD
DMA IN
SC0
SC1
MRD
MWR
/MRD
/MWR
Q
TPB
U5D
74HC00
/A15
R2
10K
C1 0.1uF
DMA OUT
INT
EF1
EF2
EF3
EF4
WAIT
CLEAR
N0
N1
N2
TPB
D2
1N4148
D1
1N4148
to/EF3 serial input 1802MC
R2A
10K
Q2
FJN3303
22K
22K
/ON
RUN
C5
4.7uF
RX
TX
R6
270
C4
4.7uF
P4
POWER+
SERIAL
R2B
10K
High for INP or OUT instruction
U5B
74HC00
U9
74LS145
I/O DECODER
P2
KEYCOL
Q1
22K
22K
FJN4303
/ON
/OFF
R5
100K
TVON
U6 74HC4040
VIDEO COUNTER
U5A
74HC00
U7 27C16 or 28C16
VIDEO SEQUENCER
U8 74HC374
VIDEO LATCH
/DMA
/INT
/BLANK
/SYNC
/EF1
RST
VSYNC
TPA
U5C
74HC00
U10
74HC244
KEYBOARD IN
R3
10K
P3
KEYROW
/EF2
/EF3
U11 74HC165
SHIFT REG
SER
QH
CLK QH
INH
SH/LD
R4
1K
P1
VIDEO
J2
KEYCOL
J3
KEYROW
SHIFT
Video levels
White 1.2V
Black 0.8v
Blank 0.4v
Sync 0v
HORIZONTAL TIMING
1802 and DOT clock=4MHz
HSYNC=DOT/256=15.625Hz
64uS/line=32 2uS bus cycle
24 DMA cycles (75%)
8 CPU bus cycles (25%)
(4 2-cycle instructions)
24 bytes/line=192 bits.
Use 192 vertical lines for "square" pixels.
RAM: 24x192=4608 bytes.
If INT handler is active during DMA (to scan keys, serial I/O, repeat lines like 1861) then Main can have 3-cycle instructions but INT overhead is 73%.
If INT handler exits when DMA starts, Main must be 2-cycle instructions but INT overhead is only 55%.
Q1-Q14 2223 2223
counter 468002468 4680024
/HSYNC
/BLANK
/DMA-OUT
SC1
8 CPU, 24 DMA cycles
VIDEO
VERTICAL TIMING
U8,U6 OUTPUTS
Q1-Q2 125 KHz
Q3 62.5 KHz
Q4 31.25KHz
Q5 15.625KHz
Q6 line 1
Q7 line 2
Q8 line 4
Q9 line 8
Q10 line 16
Q11 line 32
Q12 line 64
Q13 line 128
Q14 line 256
60Hz: 15.625KHz HSYNC / 262 lines = 59.637Hz VSYNC
50Hz: 15.625KHz HSYNC / 312 lines = 50.08Hz VSYNC
/VSYNC low on lines 0-11 (Q14=0 Q9:Q8=00,01,10)
/INT low on lines 38-39 (Q14=0 Q11=1 Q8=1 Q7=1)
Line 0-11: VSYNC, with 3 cycles inverted HSYNC.
Line 12-39: Blank (top margin).
Line 38-39: /INT=0. 69 bus cycles before 1st DMA to save regs and initialize. End with IDL to wait for DMA (allows 3-cycle instructions).
Line 40-231: DMA (192 lines of 24 DMA cycles). Also, /EF1=0 to tell Interrupt handler that DMA still in progress. Use to repeat lines to save RAM and reduce vertical resolution.
Line 232-261 (or 232-311): Blank (bot margin).
Line 262 (or 312): RST=1 to reset U6.
bottom margin->
vertical sync pulse
<-top margin
/HSYNC
/BLANK
/DMA-OUT
VIDEO
P4 Power + Serial Connector
pin 6 /ON: GND=Run +5=Reset
pin 5 TX: TTL serial out
pin 4 RX: TTL serial in
pin 3 VDD: +5 VDC
pin 2 key: (no pin)
pin 1 GND: common for +5V
U6: RST=1 on 262 60Hz Q7,Q8,Q14 or 312 50Hz Q9,Q10,Q11,Q14
U7: Program for 60Hz or 50Hz. A 4K 27C32 could have both.
U8: Bit 0,Q1,R5 latches TVON (1=video, 0=sync only). Bits 1-2 are a /4 ring counter to make Q1-Q2. Bit 7 is the VSYNC latch (1=VSYNC, 0=video, blank).
Notes:
Program U7 to account for U8 delaying /BLANK, /SYNC, /EF1, VSYNC and RST by 1 bus cycle.
Rev.B: U11-15 was hi; now low.
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Title
1802 VIP2K - VIP in an Altoids tin
Size B
Document Number C:\ORCAD\SHEET\1802\VIP2K.SCH
REV B
Date: September 12, 2018
Sheet 1 of 1